LISTING OF CLAIMS

1. (Canceled)

2. (Currently amended) The method according to claim [[1]] 8, further comprising developing the photo resist layer after exposure with both the first mask image and the second mask image.

3. (Original) The method according to claim 2, further comprising using the developed photo resist layer to protect a layer underlying the photo resist layer from at least one of etching, implantation and chemical reaction.

4. (Currently amended) The method according to claim [[1]] 8, wherein the lithography system is selected from a step-and-repeat lithography system, a step-and-scan system and combinations thereof.

5. (Currently amended) The method according to claim [[1]] 8, wherein the lithography system includes a first alignment sensor for tracking a location of the reference mark and a second alignment sensor for tracking a location of the latent image alignment mark.

6. (Canceled)

7. (Currently amended) The method according to claim [[6]] 8, wherein the enhancing includes adding a compound to the photo resist layer during photo resist formation such that the photo resist layer changes appearance in locations exposed to a threshold amount of energy as defined by the first mask image.

8. (Currently amended) A method of fabricating an integrated circuit on a wafer using dual mask exposure lithography, comprising:

forming a photo resist layer over the wafer;

aligning the wafer with respect to a lithography system using a reference mark that is formed on the wafer;

exposing the photo resist layer with a first mask image defined by a first mask using the lithography system, the first mask image including a latent image alignment mark that is transferred to the photo resist layer;

re-aligning the wafer with respect to the lithography system using the latent image alignment mark resulting from the exposure to the first mask image;

exposing the photo resist layer with a second mask image defined by a second mask using the lithography system; and

enhancing detectability of the latent image alignment mark to an alignment sensor, ~~The method according to claim 6,~~ wherein the enhancing includes developing a portion of the photo resist layer after exposure by the first mask image to establish a latent image alignment mark edge in the photo resist layer.

9. (Original) The method according to claim 8, wherein the photo resist layer includes at least two sublayers and the developed portion of the photo resist layer includes a top layer of the sublayers.

10. (Currently amended) ~~The method according to claim 1,~~ A method of fabricating an integrated circuit on a wafer using dual mask exposure lithography, comprising:

forming a photo resist layer over the wafer;

aligning the wafer with respect to a lithography system using a reference mark that is formed on the wafer;

exposing the photo resist layer with a first mask image defined by a first mask using the lithography system, the first mask image including a latent image alignment mark that is transferred to the photo resist layer;

re-aligning the wafer with respect to the lithography system using the latent image alignment mark resulting from the exposure to the first mask image; and

exposing the photo resist layer with a second mask image defined by a second mask using the lithography system;

wherein the photo resist layer includes at least two sublayers and exposure by the first mask image results in latent image alignment mark detectability in at least a top one of the sublayers.

11. (Currently amended) ~~The method according to claim 1, further comprising~~ A method of fabricating an integrated circuit on a wafer using dual mask exposure lithography, comprising:

forming a photo resist layer over the wafer;

aligning the wafer with respect to a lithography system using a reference mark that is formed on the wafer;

exposing the photo resist layer with a first mask image defined by a first mask using the lithography system, the first mask image including a latent image alignment mark that is transferred to the photo resist layer;

re-aligning the wafer with respect to the lithography system using the latent image alignment mark resulting from the exposure to the first mask image;

exposing the photo resist layer with a second mask image defined by a second mask using the lithography system; and

enhancing detectability of the latent image alignment mark by increasing exposure of the latent image alignment mark with the first mask image.

12. (Original) The method according to claim 11, wherein increasing the exposure includes exposing at least twice with the first mask.

13. (Original) The method according to claim 11, wherein increasing the exposure includes exposing with an overlapping exposure.

14. (Currently amended) ~~The method according to claim 1,~~ A method of fabricating an integrated circuit on a wafer using dual mask exposure lithography, comprising:

forming a photo resist layer over the wafer;

aligning the wafer with respect to a lithography system using a reference mark that is formed on the wafer;

exposing the photo resist layer with a first mask image defined by a first mask using the lithography system, the first mask image including a latent image alignment mark that is transferred to the photo resist layer;

re-aligning the wafer with respect to the lithography system using the latent image alignment mark resulting from the exposure to the first mask image; and

exposing the photo resist layer with a second mask image defined by a second mask using the lithography system;

wherein one of the first mask image and the second mask image defines critical dimension structures and the other of the first mask image and the second mask image defines non-critical dimension structures.

15. (Currently amended) ~~The method according to claim 1,~~ A method of fabricating an integrated circuit on a wafer using dual mask exposure lithography, comprising:

forming a photo resist layer over the wafer;

aligning the wafer with respect to a lithography system using a reference mark that is formed on the wafer;

exposing the photo resist layer with a first mask image defined by a first mask using the lithography system, the first mask image including a latent image alignment mark that is transferred to the photo resist layer;

re-aligning the wafer with respect to the lithography system using the latent image alignment mark resulting from the exposure to the first mask image; and

exposing the photo resist layer with a second mask image defined by a second mask using the lithography system;

wherein one of the first mask image and the second mask image defines edges in a first direction and the other of the first mask image and the second mask image defines edges in a second direction transverse to the first direction.

16. (Currently amended) ~~The method according to claim 1, further including~~ A method of fabricating an integrated circuit on a wafer using dual mask exposure lithography, comprising:

forming a photo resist layer over the wafer;

aligning the wafer with respect to a lithography system using a reference mark that is formed on the wafer;

exposing the photo resist layer with a first mask image defined by a first mask using the lithography system, the first mask image including a latent image alignment mark that is transferred to the photo resist layer;

re-aligning the wafer with respect to the lithography system using the latent image alignment mark resulting from the exposure to the first mask image;

exposing the photo resist layer with a second mask image defined by a second mask using the lithography system; and

at least partially developing the photo resist layer between exposing with the first mask image and the second mask image.

17. (Currently amended) The method according to claim [[1]] 8, wherein the first mask image and the second mask image create a composite mask image on the photo resist layer.

18-23. (Canceled)